29C95

Multi-Channel ECMA 102/V110 Protocol Controller

Description

The MHS 29C95 is a multi-channel data link protocol controlller device. It multiplexes/demultiplexes up to 32 full duplex data channels to support implementation of data links based on either the ECMA 102/V110 protocol or clear channel mode.

The device operates at layer 2 of the OSI (Open System Inteconnection) model as described by ISO (International Organization for Standatdization). It resides between L.I.U and framer PCM devices such as, respectively, the MHS 29C3XX and 29C96 and a memory shared with a system host microprocessor (see typical application fig.1).

The 29C95 processes transmit and receive data on a PCM communication medium in either CEPT (2.048 bps) or T1/DS1 (1.544 Mbps) framing format. The device provides ECMA 102 formatting/extract functions for asynchronous data. It manages, for each of the active data channels, access to buffers into the shared memory.

Provisions to operate in clear channel, non ECMA 102 mode, are readily available and can be programmed on any channel independently of every other.

The cicuit is entirely compatible with ISDN specified by CCITT and supports connections of terminals through the ISDN at the primary rate in ECMA 102 format. It also supports mode 0, 1, 2 and 3 of the DMI protocol for clear channel transmission of data at 64 kbps.

The 29C95 finds application in several areas of telecommunication, including multimedia terminals and concentrators, MUX, etc.

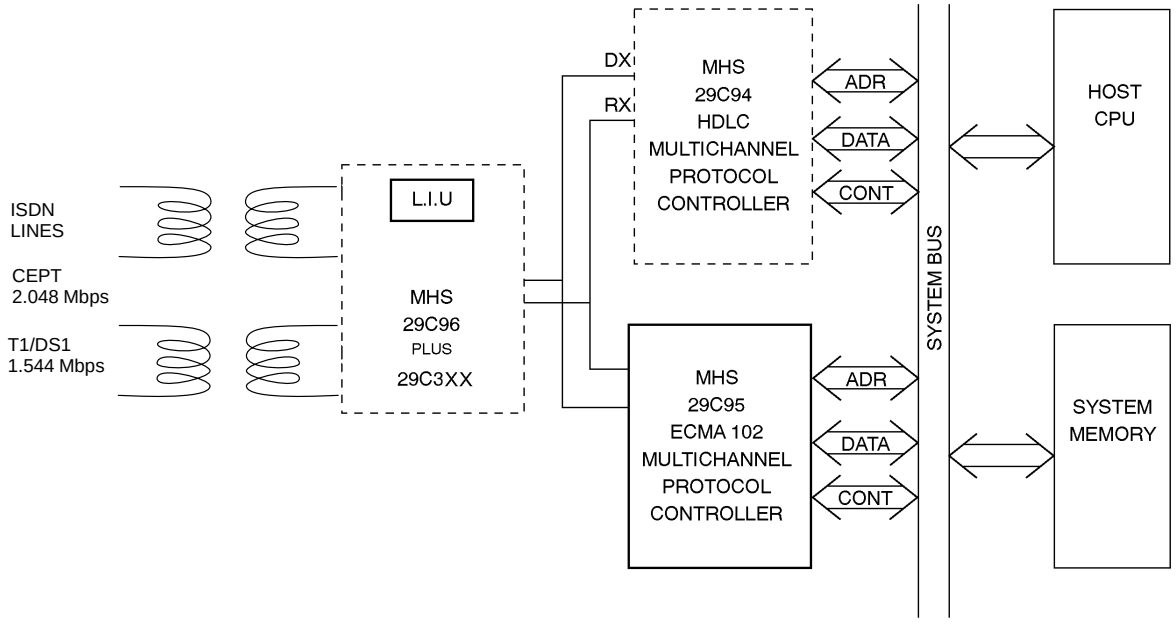
Features

- Single chip one micron CMOS monolithic device simplifies ISDN/DMI implementation
- Compatible with 2.048 Mbps CEPT and 1.544 Mbps T1/DS1 ISDN framing format
- Provides ECMA 102 formatting and clear channel transmission for up to 32 full duplex channels
- Dynamic channel allocation allowing, in clear channel mode, any user defined hyper channel including H_0, H_{11} and H_{12}
- Programmable number of channel from 2 to 32, with loop back mode for test purposes
- Asynchronous 7 bit/8 bit characters processing handling both 1 bit and 2 bit stops
- Programmable parity check independent, per channel, programmable transmitting and receiving data rate from 600 up to 19200 bauds
- Programmable automatic in band connect/disconnect
- Independent, per channel, receiving/transmitting data rate as well as channel valid/not valid
- Capability of data receiving at over baud rates
- Break character detection
- Burst data collection upon CPU request on every channel
- On chip receive and transmit context saving as well as buffer memory management
- Independent, per channel, receiving and/or transmitting status report
- Compatible with both MOTOROLA 680X0 and INTEL 80X86 CPU series
- On chip crystal oscillator (33 MHz)
- Operates from a single 5 V power supply
- Packaged in 68 pin PLCC

Interface

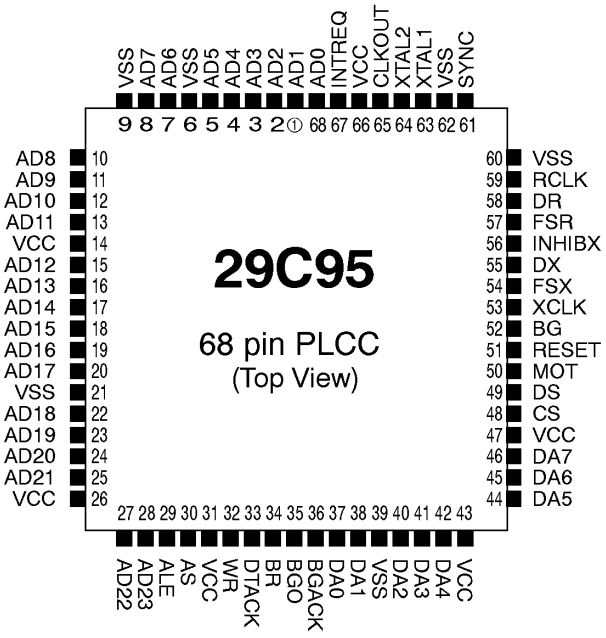
Block Diagram

Figure 1.



Pin Configuration

Figure 2.



Pin Description

Pin	Symbol	Type	Description
1	AD1	I/O	Address bus bit 1.
2	AD2	I/O	Address bus bit 2.
3	AD3	I/O	Address bus bit 3.
4	AD4	I/O	Address bus bit 4.
5	AD5	I/O	Address bus bit 5.
6	VSS	SUPPLY	GROUND
7	AD6	I/O	Address bus bit 6.
8	AD7	I/O	Address bus bit 7.
9	VSS	SUPPLY	GROUND
10	AD8	I/O	Address bus bit 8.
11	AD9	I/O	Address bus bit 9.
12	AD10	I/O	Address bus bit 10.
13	AD11	I/O	Address bus bit 11.
14	VCC	SUPPLY	5 V supply
15	AD12	I/O	Address bus bit 12.
16	AD13	O	Address bus bit 13.
17	AD14	O	Address bus bit 14.
18	AD15	O	Address bus bit 15.
19	AD16	O	Address bus bit 16.
20	AD17	O	Address bus bit 17.
21	VSS	SUPPLY	GROUND
22	AD18	O	Address bus bit 18.
23	AD19	O	Address bus bit 19.
24	AD20	O	Address bus bit 20.
25	AD21	O	Address bus bit 21.
26	VCC	SUPPLY	5 V supply
27	AD22	O	Address bus bit 22.
28	AD23	O	Address bus bit 23.
29	ALE	I/O	Address latch enable. active high. (used in INTEL mode). must be tied to ground in MOTOROLA mode
30	AS	I/O	Address strobe active low (MOTOROLA mode) RD active low (INTEL mode)
31	VCC	SUPPLY	5 V supply
32	WR	I/O	Write strobe active low
33	DTACK	I/O	R/W cycle acknowledge. Active low (MOTOROLA mode) active high (INTEL mode) Output in slave mode, input in master mode (DMA mode)
34	BR	O	Bus request. Active low (open collector) Daisy chain output. active low when BG is active and when there is no
35	BGO	O	internal bus request (MOTOROLA mode only) Bus grant acknowledge. active low (MOTOROLA mode).
36	BGACK	I/O	DAISY CHAINED Bus request input. active low (INTEL mode). Data bus bit 0.
37	DA0	I/O	Data bus bit 1.
38	DA1	I/O	GROUND
39	VSS	SUPPLY	Data bus bit 2.
40	DA2	I/O	Data bus bit 3.
41	DA3	I/O	Data bus bit 4.
42	DA4	I/O	5 V supply
43	VCC	SUPPLY	Data bus bit 5.
44	DA5	I/O	Data bus bit 6.
45	DA6	I/O	Data bus bit 7.
46	DA7	I/O	5 V supply
47	VCC	SUPPLY	
48	CS	I	Chip select active low
49	DS	I	Data strobe active low (MOTOROLA mode only).
50	MOT	I	MOTOROLA/INTEL mode selection (active high for MOTOROLA mode active low for INTEL mode).
51	RESET	I	RESET active low (MOTOROLA mode), active high (INTEL MODE).
52	BG	I	Bus grant. active low (MOTOROLA mode) active high (INTEL mode).

Pin Description (continued)

Pin	Symbol	Type	Description
53	XCLK	I	Bit clock transmit (2 048 kHz or 4 096 kHz CEPT mode 1 544 kHz or 4 088 T1/DS1 mode)
54	FSX	I/O	Frame sync transmit (8 kHz) input active high in slave mode output active high in master mode.
55	DX	O	DATA transmit
56	INHIBX	O	Indicate that the current transmit time slot is inhibited. active high.
57	FSR	I/O	Frame sync RECEIVE (8 kHz) input active high in slave mode output active high in master mode.
58	DR	I	DATA receive
59	RCLK	I	Bit clock receive (2 048 kHz or 4 096 kHz CEPT mode 1 544 kHz or 4 088 T1/DS1 mode)
60	VSS	SUPPLY	GROUND
61	SYNC	I	Input indicate that the PCM receiver is synchronized (normally output of a framer) active high
62	VSS	SUPPLY	GROUND
63	XTAL1	I	Main clock input or oscillator input (25 to 33 MHz).
64	XTAL2	O	oscillator output
65	CLKOUT	O	Buffered output of main clock
66	VCC	SUPPLY	5 V supply
67	INTREQ	O	Interrupt request active high.
68	AD0	I/O	Address bus bit 8.

Functional Description

General Description

The 29C95, multi-channel ECMA 102 protocol controller, transmits data to and receives data from a Line Interface Unit (L.I.U) made of a PCM transceiver and a framer devices, such as the MHS 29C300 and MHS 29C96. Data are received/transmitted at the ISDN/DMI primary rate (2.048/1.544 Mbps).

It stores and fetches the data to and from memory buffers allocated into an external memory shared with the system host microprocessor as illustrated on figure 1.

The 29C95 multiplexes/demultiplexes up to 32 full duplex channels over the time slots of the ISDN PCM frame. In clear channel transmission mode, two or more, adjacent or non adjacent, channels may be concatenated to form an hyperchannel.

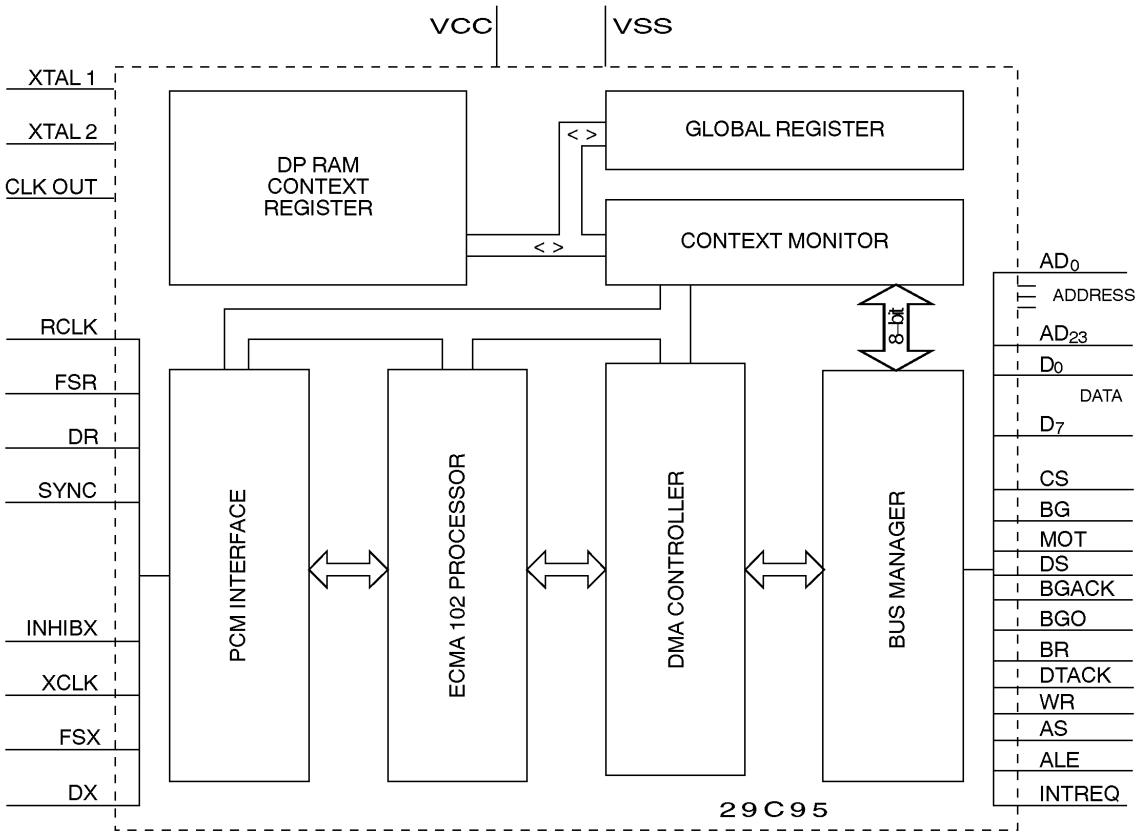
Data to be transmitted are fetched in 8 bit parallel form from the allocated buffers, one channel after the other, through DMA cycles. They are processed to achieve data frame protocol formatting and, if required, rate adaptation, then transmitted serially to the PCM data link.

Conversely, the incoming stream of serial data is processed, channel after channel, to get rate adaptation and data frame protocol deformatting. Received data are stored in byte form into the channel allocated buffers trough DMA cycles.

Each channel is allocated 8 buffers for the data to be transmitted and 8 buffers for data being received. Every buffer has a 64 kbytes capacity. The 29C95 internal DMA CONTROLLER has an addressing capability of up to 512 buffers, 256 for receiving data and 256 for transmitting.

Every channel is processed according operating modes specified by the host CPU that initializes the 29C95 and sets up the internal control registers, which in turn control the internal logic of the chip as shown on the 29C95 block diagram of figure 3. Two types of operating modes, Global Mode and Channel Mode, are programmable and are being set up by the host CPU.

Figure 3. Block Diagram.



The Global Mode applies to all channels at the same time. Programming of Global Mode selects operations according to table 1 below.

Within the Global Mode, per channel operating mode must be specified on any channel independently of every other. Furthermore, on any channel, the receiving mode is independent of the transmitting one. For both, transmitting and receiving sides, the programmable Channel Mode parameters are as shown on Table 2.

Table 1 : Global Mode Programming.

CEPT 32 channels	Vs	T_1/DS_1 24 channels
Test mode	Vs	CEPT & T_1/DS_1 modes
PCM slave mode	Vs	PCM master mode
PCM single clock	Vs	PCM double clock (GCI mode)
All channels valid	Vs	All channel not valid
PCM frame synchronization offset control		
Loop back mode for test purposes.		

Table 2 : Channel Mode Programming.

ECMA 102 mode	Vs	Clear channel mode
Time slot valid	Vs	Time slot not valid
Channel number (1)		
Rate adaptation		
Buffer descriptors -Processing status		
– Buffer size/word count (16 bits)		
– Start adress (24 bits)		
TRANSMIT ONLY		**RECEIVE ONLY**
One bit parity valid		One bit parity valid
Odd/even parity select		Odd/even parity select
7 bit/8 bit character select		7 bit/8 bit character select
Data bit repetition rate		Data bit repetition rate
1-stop bit/2-stop bit select		For test purpose, enforces synchronization of 80 bit frame machine.
One bit allowing to use the x-bit from the receiving side to inhibit the transmit DMA requests.		
x bit to be transmitted.		
Disconnect control command.		
Enforces S_A-S_B bits transmission.		
Value of S_A-S_B bits when enforcing bit is true.		

(1) Identical numbers for the logical channel and current time slot reference means that this is either a single channel or the head of an hyperchannel. If the logical channel number is equal to another time slot reference, then the current time slot must be concatenated to the referenced one, wether it is adjacent or not.

Receiving and transmitting parameters that are specific to a channel and that control the processing of data during one time slot, are usually referred as the “TIME SLOT CONTEXT” or, in short, “CONTEXT”. Contexts are stored into the device internal registers, made of a dual port RAM that is accessed by the “CONTEXT MONITOR” functional block.

The internal operations of the 29C95, controlled by the registers, are partitionned into five major logic blocks as shown figure 3. The blocks are :

1. - CONTEXT MONITOR
2. - PCM HANDLER
3. - ECMA 102 PROCESSOR
4. - DMA CONTROLLER
5. - BUS MANAGER

In summary, on each successive time slot of the PCM frame and within the functional Global Mode, specific time slot context is restored from dedicated registers at the beginning of the time slot. Then processing actions take place upon the time slot duration according to the controlling parameters of the context, which is updated and saved at the end of the time slot until its next occurence, on the following PCM frame, 125µs later.

On any time slot (about 3.9 µs for the CEPT frame), assuming that it is valid and that there are valid data being transmitted and received, a lot of discrete actions must take place over its duration: i.e. 28 bytes of context to restore then save, data byte to fetch and store, parity checking computation, serialization and/or deserialization of data, etc.

To do so, the 29C95 operates at an internal frequency of up to 33 MHz (30 ns clock period) driven either by an external clock or by an internal crystal oscillator. Furthermore, the 29C95 uses throughout its synchronous design a pipelined architecture that results in introducing quantified delay between the time a data byte is fetched into a buffer until it is serially output on the dx pin. Equivalent, but not equal, delay exists on the receiving side. In both cases. Functional operations of the main logic blocks are summarized thereafter.

Logic Block Description

Context Monitor

The CONTEXT MONITOR performs context switching from one time slot to the next. A three stage pipeline is used for the process of context restore-execute and update-save. It also provides the bus manager access to the dual port RAM/control registers.

Table 3 : Three Stage CONTEXT MONITOR Pipeline.

Steps	Time slot N – 1	Time slot N	Time slot N + 1
1. Read context	Time slot N	Time slot N+1	Time slot N + 2
2. Execute context	Time slot N – 1	Time slot N	Time slot N + 1
3. store context	Time slot N – 2	Time slot N – 1	Time slot N

PCM Handler

The PCM HANDLER receives serial data from the PCM link via the Line Interface Unit. It performs receive and/or transmit data synchronization and supplies a bit clock to the ECMA102 PROCESSOR. It also generates an internal reference “bit 0/Time slot 0” according frame sync. offset programming. The PCM HANDLER may operate in either slave or master mode. In slave mode, the frame synchronization signals FSX/FSR are input, while in master mode, FSX/FSR are output. In any event the bit-clock XCLK/RCLK are input only.

ECMA 102 Processor

The ECMA102 PROCESSOR logic block receives the data to be transmitted from the DMA CONTROLLER in 8 bit parallel form and send them serially to the PCM INTERFACE. Conversely, on the receiving side, the ECMA102 processor receives serial data from the PCM INTERFACE and sends them in byte form to the DMA CONTROLLER.

Transmitting functions

The ECMA 102 PROCESSOR generates the ECMA 102 frame skeleton. It performs ECMA 102 protocol formatting with S_A, S_B, X, E_i and stop bit insertion under channel control. It also performs bit repetitions to ensure rate adaptation, computes, if necessary, the parity check bit and formats data into either 7-bit or 8bit characters.

Receiving functions

The ECMA 102 PROCESSOR ensures data synchronization versus the ECMA 102 frame. It sorts out the frame bits and data bits, unformats the data characters to put them in byte form with the parity check bit. It also detects the BREAK character and supplies the S_A-S_B-X-E_1-E_2-E_3 bit status.

DMA Controller

Transmitting functions

The DMA CONTROLLER fetches data from the buffers through the BUS MANAGER according a handshake scheme. It supplies the data to the ECMA 102 PROCESSOR and updates the current buffer address and word count.

Receiving functions

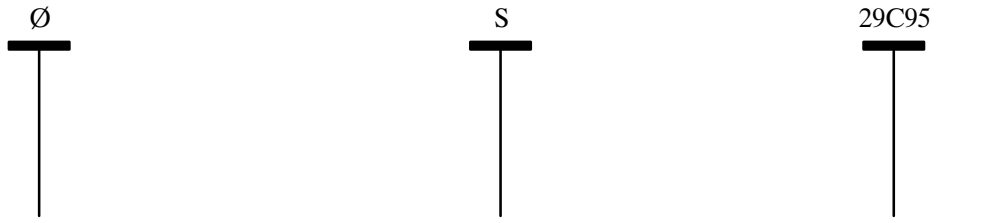
The DMA CONTROLLER gets the data from the ECMA 102 PROCESSOR and stores them through the bus manager into a buffer. It also updates word count and address pointer of current buffer. Upon cpu control, the BUS MANAGER executes a burst of data collect on every channel.

Bus Manager

Interfaces the 29C95 and the host system bus. Generates bus request. Controls the bus when granted. Performs daisy chain arbitration. Initiates an interrupt request to report errors or data frame completion on any time slot for both transmit and receive.

A fully comprehensive data sheet of the 29C95 is available on request. It includes the necessary registers descriptions and mapping and other relevant information so that the MHS 29C95 may be used to its full efficiency.

Ordering Information



TEMPERATURE RANGE
Ø COMMERCIAL 0 TO 70 °C
I INDUSTRIAL −40 TO 85 °C

PACKAGE : S = PLCC

Part number
29C95

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